REMARKS

The amendment to the specification corrects an obvious typographical error.

Applicant respectfully requests that the finality of the Office action dated 12 May 2005 be withdrawn and the instant Amendment entered as a matter of right. In the 12 May 2005 Office action the Examiner asserts that "additional explanation is given within the body of the art rejection for applying the Nakamura reference, however, neither the reference used nor the legal basis for the rejection have been changed." It may be true that the reference (Nakamura) and the legal basis (§102) for the rejection have not been changed. However, the supposed "additional explanation" is in fact, a completely new factual basis for the ground of rejection. It is respectfully submitted that when an entirely different portion of an existing reference is provided to support a ground of rejection, fairness dictates that the applicant have an opportunity to respond. Application of Rudolf Weichert, 54 CCPA 957, 370 F.2d 927 (CCPA 1967).

Furthermore, applicant completely and fully responded to the first Office action which should have been a complete examination of the pending claims. The Office no longer relies upon the earlier cited paragraphs to support its grounds of rejection. For example, in the first Office action claim 1 was rejected on the basis of paragraph 10 of Nakamura whereas in the final Office action, claim 1 is rejected on the basis of paragraphs 69-77 of Nakamura. Applicant fully responded to the ground of rejection set forth in the first Office action, and that rejection, at least so far as it was based on paragraph 10, has not been repeated. Accordingly, that rejection, insofar as it is based on paragraph 10, has been withdrawn. Applicant must now respond to a new ground of rejection based on paragraphs 69-77. Applicant did not amend claim 1, and therefore the substitution of paragraphs 69-77 to support a §102 rejection cannot be said to have been necessitated by applicant's amendments. Applicant should have received a full examination based on Nakamura in the first Office action, and if the Office intended to rely upon paragraphs 69-77, such reliance should have been set forth. Applicant should not now be required to file either an appeal or an RCE to respond to the new grounds of rejection. Accordingly, applicant respectfully requests that the finality of the instant Office action be withdrawn and that the instant amendment be entered as a matter of right.

Alternatively, it is respectfully requested that the instant amendment be entered as it places the claims in better condition for appeal. Inasmuch as applicant is responding to new grounds of rejection, it is clear that applicant could not have submitted these amendments or remarks earlier.

In paragraph 7 of the Office action, claim 1 is rejected on the basis of Nakamura, Figure 6-7 and paragraphs 0069-0070. It is the Office's position that "the refresh operation is performed using a refresh address counter without supplying the address to the buffer of the memory array for each cell of the

array". It is known in the art for memory devices to have internal refresh address counters or other control circuits. Claim 1 has been amended to recite that the memory array is operable to function without at least one of a precharge signal, a row address latch signal, and a column address latch signal "during read and write operations". The Office has failed to demonstrate that the amended claim, as a whole, is anticipated by Nakamura. Accordingly, it is respectfully requested that the rejection of claim 1, as well as its dependent claims 2-5, be withdrawn.

In paragraph 8 of the Office action, claim 6 stands rejected for substantially the same reasons advanced with respect to claim 1. Accordingly, claim 6 has been amended to add the language "during read and write operations". For the same reasons set forth with respect to claim 1, it is respectfully submitted that the rejection of claim 6, as well as its dependent claims 7-10, be reversed.

In paragraph 9 of the Office action, claim 11 stands rejected in view of Nakamura, specifically Figure 2, paragraphs 0056-0061. It is the Office's position that "Figure 2 shows each memory bank of the memory array has a memory controller, element 26". Although each memory bank has a controller 26, it is seen that command decoder 13, refresh address counter 22, address buffer 14, I/O buffer 16, the command input buffer and the clock input buffer are common for all of the banks. That should be contrasted with applicant's Figure 5 in which duplicate circuitry is provided for each bank. Thus, it is respectfully submitted that claim 11, which recites that each of the memory banks is "independently connected to one of said plurality of controllers, each of said controllers being independently connected to a processor" has not been shown to be disclosed by Nakamura Figure 2 which requires that a substantial number of components be used in common amongst the memory banks. For that reason, it is respectfully requested that the rejection of claim 11, as well as its dependent claims 12-17, be withdrawn.

In paragraph 10 of the Office action, claim 18 stands rejected under Nakamura for substantially the same grounds as the rejection of claim 11. For the reasons set forth above, it is respectfully submitted that claim 18 has not been demonstrated to be anticipated by Nakamura. Accordingly, it is respectfully submitted that the rejection of independent claim 18, as well as the rejection of its dependent claims 19-24, should be withdrawn.

In paragraph 11 of the Office action, claim 25 stands rejected in view of Nakamura. It is respectfully submitted that none of the cited portions of Nakamura teach a plurality of memory arrays directly connected to the processor. The portions of Nakamura cited are directed to the refresh operation using a refresh address counter and do not disclose, or even suggest, that the plurality of transparent SDRAM arrays be directly connected to the processor. For those reasons it is respectfully requested that the rejection of independent claim 25, and its dependent claims 26-30, be withdrawn.

In paragraph 12 of the Office action, claim 31 stands rejected as being anticipated by Nakamura for substantially the same reasons set forth with respect to claim 25. Again it is reiterated that the cited portions of Nakamura do not disclose or suggest a transparent SDRAM having a plurality of memory banks, with each of the plurality being directly connected to the processor. Rather, as seen clearly from Figure 2 of Nakamura, each of the banks shares common circuitry between the bank and the processor. Accordingly, it is respectfully submitted that the rejection of independent claim 31, as well as the rejection of its dependent claims 32-36, must be withdrawn.

In paragraph 13 of the Office action, claim 37 stands rejected in view of Nakamura. It is the Office's position that Figure 2 "shows each memory bank of the SDRAM has a command latch circuit for supplying the commands to the banks of the array. A refresh command is sent to each individual controller for each memory bank". The Examiner ignores, however, that the command latch 24 for each of the banks is responsive to a common command decoder 13. Thus, the Office has not demonstrated that the banks may be simultaneously accessed. Contrast Figure 2 of Nakamura with Figure 5 of Applicant's disclosure. For the foregoing reasons it is respectfully submitted that the rejection of independent claim 37, as well as the rejection of its dependent claims 39-42, must be withdrawn.

Claim 43 stands rejected in view of Nakamura in paragraph 14 of the Office action for substantially the same reasons set forth above. More particularly the Office relies upon Figure 2 of Nakamura, element 26. The controller 26 is a device internal to the banks of Nakamura and is not the same as the processor 36 shown in Applicant's Figure 3. It is respectfully submitted that applicant has demonstrated that the Office has failed to make a *prima facie* showing that the banks of Nakamura may communicate with a processor 36 of the type shown in applicant's Figure 3 in a simultaneous manner. Therefore it is respectfully submitted that the rejection of claim 43, as well as the rejection of its dependent claims 44-48, must be withdrawn.

With respect to paragraph 15 of the Office action and claim 49, applicant submits that the Office has not demonstrated that the banks of Nakamura may be simultaneously accessed. Accordingly, it is respectfully submitted that the rejection of independent claim 49, and its dependent claims 50 and 51, must be withdrawn.

In paragraph 16 of the Office action, independent claim 52 stands rejected in view of Nakamura. The Office again relies upon Nakamura as teaching a refresh operation for maintaining data in a power down mode without input from a programmer or a system designer. However, claim 52 is directed to a simultaneous reading operation and a simultaneous writing operation. It is not seen how the refresh mode of Nakamura anticipates a simultaneous read/write operation. Accordingly, it is respectfully submitted

that the Office has failed to demonstrate that Nakamura anticipates claim 52. It is respectfully submitted that the rejection of independent claim 52, as well as its dependent claims 53-58, must be withdrawn.

Applicant has made a diligent effort to place the claims in condition for allowance. Accordingly, a Notice of Allowance for claims 1 – 58 is respectfully requested. If the Examiner is of the opinion that the instant application is in condition for disposition other than through allowance, the Examiner is respectfully requested to contact applicants' attorney at the telephone number listed below so that additional changes may be discussed.

Respectfully submitted,

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